UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,254	01/02/2002	Roni Rosner	042390.P12485	9368

8791 7590 09/29/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
KISS, ERIC B	
ART UNIT	**PAPER NUMBER**
2192	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,254	ROSNER ET AL.	
	Examiner	Art Unit	
	Eric B. Kiss	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-25 and 27-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-25 and 27-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20050906*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6 September 2005 has been entered.

Information Disclosure Statement

2. The information cited in the information disclosure statement filed 6 September 2005 has been considered.

Response to Arguments

3. Applicant's arguments filed 4 November 2004 have been considered and responded to as set forth in the Office action mailed 6 April 2005. As Applicant has not submitted new arguments, the Examiner maintains the position taken in the previous Office action.

Claim Objections

4. Claim 27 is objected to because of the following informalities: "flags based" in line 3 of claim 27 should presumably read --flags are based--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation "The method of claim 5" in line 1. There is insufficient antecedent basis for this limitation in the claim. In the interest of compact prosecution, claim 6 is subsequently interpreted as being dependent from claim 2, rather than from canceled claim 5, for the purpose of further examination.

Claim Rejections - 35 USC § 102

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 1, 7, 8, 25, 28, and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No 5,802,373 to Yates et al.

As per claim 1, *Yates et al.* disclose receiving a binary of a program code, the binary based on a first instruction set architecture (see, for example, the Abstract); translating the binary, wherein the translated binary is based on a combination of the first instruction set

architecture and a second instruction set architecture (see, for example, the Abstract); and executing the translated binary (see, for example, the Abstract).

The translated binary of *Yates et al.* is **based on** a combination of the first instruction set architecture and a second instruction set architecture. As the pre-translation instructions were designed for the first instruction set architecture, the resulting post-translation instructions are **based on** (or derived from) those instructions and thus, **based on** (or derived from) the first instruction set architecture. Additionally, the translated code is **based on** the second (native) instruction set architecture, as this is a form that is directly executable (see *Yates et al.*, Abstract).

As per claim 7, *Yates et al.* further disclose the first instruction set architecture comprising floating-point instructions and wherein the second instruction set architecture comprises floating-point instructions, wherein the translating of the binary comprises translating the floating-point instructions of the first instruction set architecture to the floating-point instructions of the second instruction set architecture (see, for example, col. 47, lines 1-4).

As per claim 8, *Yates et al.* further disclose the translating of the binary comprising storing a portion of a hardware stack in a register of a processor translating the binary (see, for example, col. 46, lines 57-67).

As per claims 25 and 28, these are machine-readable medium claims substantially parallel to the claimed methods discussed above (claims 1 and 7, respectively). *Yates et al.* further disclose the use of such a machine-readable medium for implementing the prescribed methods (see, for example, Fig. 1), and all other limitations have been addressed as set forth above.

As per claim 29, *Yates et al.* further disclose, in the case of self modifying code, the translating of the binary to include an instruction to controllers of memories that store the binary to perform write operations independent of whether the write operations modify a location where the binary is stored (see, for example, col. 10, lines 49-53).

Claim Rejections - 35 USC § 103

9. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

10. Claims 2-4, 6, 9, 11-24, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No 5,802,373 to Yates et al. in view of U.S. Patent No. 6,496,922 to Borrill.

As per claim 2, *Yates et al.* disclose receiving a binary of a program code, the binary based on a first instruction set architecture (see, for example, the Abstract); translating the binary, wherein the translated binary is based on a combination of the first instruction set architecture and a second instruction set architecture (see, for example, the Abstract); and executing the translated binary (see, for example, the Abstract). *Yates et al. fail* to expressly disclose checking instruction set architecture execution flags, the instruction set architecture execution flags to indicate at least one translation of a portion of the binary. However, *Borrill* teaches the use of instruction set architecture execution flags (an ISA tag) indicating the native ISA for "visiting" code (see, for example, col. 2, line 58, through col. 3, line 11; and col. 4, lines 30-58). *Borrill* teaches multiple ISA execution flags. A tag is read for each of a plurality of

instructions (see *Borrill*, col. 4, lines 30-62). Further, the fuction of the Dynamic Decode Unit (DDU) of *Borrill* is to translate non-native instructions (see *Borrill*, col. 5, lines 19-30). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of *Yates et al.* to include such checking of instruction set architecture execution flags as per the teachings of *Borrill*. One would be motivated to do so to reduce overhead associated with translating and processing non-native instructions and facilitate easier incorporation of non-native instructions into executable code.

As per claim 3, in addition to the disclosure and teaching applied above to claim 2, *Borrill* further teaches the instruction set architecture execution flags being set by a programming environment of the binary (see, for example, col. 2, line 58, through col. 3, line 11; and col. 4, lines 30-58). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of *Yates et al.* to include such setting of architecture execution flags as per the further teachings of *Borrill*. One would be motivated to do so to assign meaningful instruction identifiers recognizable by the native system.

As per claim 4, in addition to the disclosure and teachings applied above to claim 2, *Borrill* further teaches a register in a processor translating the binary being to store the instruction set architecture execution flags (see, for example, col. 4, lines 15-29). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of *Yates et al.* to include such storing/processing of architecture execution flags as per the further teachings of *Borrill*. One would be motivated to do so to as a necessary means of implementing and executing such instructions.

As per claim 6, in addition to the disclosure and teachings applied above to claim 2, *Borrill* further teaches the translating and executing being based on a command, the instruction set architecture execution flags based on a number of command line flags associated with the command (see, for example, col. 2, line 58, through col. 3, line 11; and col. 4, lines 30-58). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the method of *Yates et al.* to include such command line flags as per the further teachings of *Borrill*. One would be motivated to do so to reduce overhead associated with translating and processing non-native instructions and facilitate easier incorporation of non-native instructions into executable code.

As per claim 9, *Yates et al.* disclose receiving a binary of a program code, the binary based on a first instruction set architecture (see, for example, the Abstract); and executing the binary, wherein the executing comprises translating at least one instruction of the binary based on the first instruction set architecture to at least one instruction based on a second instruction set architecture, wherein the translated binary is based on a combination of the first instruction set architecture and a second instruction set architecture (see, for example, the Abstract); and executing the translated binary (see, for example, the Abstract). *Yates et al. fail* to expressly disclose checking instruction set architecture execution flags, the instruction set architecture execution flags to indicate at least one translation of a portion of the binary. However, *Borrill* teaches the use of instruction set architecture execution flags (an ISA tag) indicating the native ISA for "visiting" code (see, for example, col. 2, line 58, through col. 3, line 11; and col. 4, lines 30-58). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of *Yates et al.* to include such checking of instruction

set architecture execution flags as per the teachings of *Borrill*. One would be motivated to do so to reduce overhead associated with translating and processing non-native instructions and facilitate easier incorporation of non-native instructions into executable code.

As per claim 11, *Yates et al.* further disclose, in the case of self modifying code, the translating of the binary to include an instruction to controllers of memories that store the binary to perform write operations independent of whether the write operations modify a location where the binary is stored (see, for example, col. 10, lines 49-53). Therefore, for reasons stated above, such a claim also would have been obvious.

As per claim 12, *Yates et al.* further disclose the second instruction set architecture having an address space that is larger than the first instruction set architecture, the translating of the binary comprising using the address space of the second instruction set architecture (see, for example, col. 83, lines 56-65). Therefore, for reasons stated above, such a claim also would have been obvious.

As per claim 13, in addition to the disclosure applied above to claim 12, *Yates et al.* fail to expressly disclose data accessed by the binary being stored in a single segment in memory and wherein an offset value for translating a virtual address to a physical address for the data is not modified during execution of the binary. However, *Borrill* teaches such handling of non-native addressing without modifying the non-native offset address (see, for example, col. 6, line 64, through col. 7, line 24). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of *Yates et al.* to include such non-native offset address handling as per the teachings of *Borrill*. One would be motivated to do so

to provide simplified support and proper emulation for non-native instructions relying on a smaller address space.

As per claims 14-18, these are system claims substantially parallel to the claimed methods discussed above (claims 9, 4, 3, 12, and 13, respectively). *Yates et al.* further disclose a system for implementing the prescribed methods (see, for example, Fig. 1), and all other limitations have been addressed as set forth above. Therefore, for reasons stated above, such claims also would have been obvious.

As per claims 19-24, these are apparatus claims substantially parallel to the claimed methods discussed above (see claims 4, 7, 8, and 11-13, respectively). *Yates et al.* further disclose an apparatus for implementing the prescribed methods (see, for example, Fig. 1), and all other limitations have been addressed as set forth above. Therefore, for reasons stated above, such claims also would have been obvious.

As per claim 27, this is a machine-readable medium claim substantially parallel to the claimed method discussed above (claim 6). *Yates et al.* further disclose the use of such a machine-readable medium for implementing the prescribed methods (see, for example, Fig. 1), and all other limitations have been addressed as set forth above. Therefore, for reasons stated above, such a claim also would have been obvious.

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No 5,802,373 to Yates et al. in view of Bich C. Le, "An Out-of-Order Execution Technique for Runtime Binary Translators," 1998 (hereinafter *Le*).

As per claim 10, in addition to the disclosure applied above to claim 9, *Yates et al.* fail to expressly disclose the first instruction set architecture including in-order access to memory and the second instruction set architecture including out-of-order accesses to memory, the translating of the binary to include out-of-order accesses to memory by a processor executing the binary. However, *Le* teaches a runtime binary translator environment which facilitates out-of-order processing in the translated code (see, for example, sections 1.1 and 1.2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of *Yates et al.* to include out-of-order accesses to memory as per the teachings of *Le*. One would be motivated to do so to achieve higher performance.

Conclusion

12. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Eric B. Kiss whose telephone number is (571) 272-3699. The Examiner can normally be reached on Tue. - Fri., 7:00 am - 4:30 pm. The Examiner can also be reached on alternate Mondays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Tuan Dam, can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature should be directed to the TC 2100 Group receptionist: 571-272-2100.

EBK /EBK
September 20, 2005

TUAN DAM
SUPERVISORY PATENT EXAMINER